

ABSTRACT

Method and apparatus for efficiently analyzing visual defects of an integrated circuit wafer in the manufacturing process thereof by utilizing an asymmetric visual defect review methodology that can effectively extract high yield-killing defects out of numerous reported defects within the limited capacity and manpower available for review. Roughly described, the method comprises inspecting the semiconductor wafer, thereby obtaining the defect location and defect size, sampling the defects asymmetrically by determining asymmetrical defect review ratios, and thereby reviewing the defects asymmetrically. Also described is a method of asymmetrically sampling visual defects that can effectively extract out high yield-killing defects from a mass of defects by determining asymmetric defect review ratios, and a system for use in sampling visual defects asymmetrically.